Pano Upper Board Schematic

Page	Description
1	Title Page
2	Video DAC
3	USB Host Controller
4	USB Interface
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8	Power Supply Monitoring
9	FPGA Configuration
10	FPGA Debug & Pixel Clock
11	FPGA Power and Decoupling
12	DDR DRAM Interface
13	Connection to Lower Board

Rev	Date	Pages	Description of Changes
00	1/26		Release to Fab
	2/9	9	Fix FAN1117 resistor positions
		7	Fix Ethernet strapping/LED circuit
		11	Fix Dip Switch high side voltage to 1.8V
	2/19	11	Ground Mounting holes
		8	Remove RS232 serial port
		6	Remove Smart Card Feature
	2/22	8	Remove PS/2 ports
		4,5,12	Sub Alum Electrolytic Capacitors for cost
		10	Sub switch for jumper
		6	R2R Resistive DAC experiment
		7	Move position of TXC series termination and change name
	2/26	9	Remove linear regulator for Video AVDD Downsize 1.8V & 2.5V linear regulators
		12	Downsize capacitors around FPGA (100uF -> 10uF)
		2	Replace ferrites on synch signals with resistors
		7	Remove R56 and R59 (previously DNS)
		8	Replace PS/2 ports
	2/27	4,10,11	New LED symbol to flip device
		numerous	Update FPGA symbol pins
	2/28	numerous	Update FPGA symbol pins
	3/1	10	add back the jumper
		8	correct typo in R2R DAC
		3	Remove pullups on rdn,wrn
		2	gnd or tie vcc various pins (remove resistors) on THS8135
		11	reduce resistor value on LEDs
	3/7	11	change to 1208 right angle LEDs
		2	add pullup to FPGA side of DDC SDA, change to 4.7k values
		8	add pullup to SDA to clock synthesizer
	3/8	10	add stake pins to allow spi prog after snap off removed
	3/9	4	change cap shape name to c size
		11	add third mech. pad for SMT right angle LED
	3/11	11	change clock PLL to use OUT2
		7	change 100mhz osc series term to 0 ohms
		13	remove series terms on address/cmd bus to DDR
	3/11	3	connect ISP1760 REV5V to V5V0
		3	Remove ferites on isp1760 rref per more recent app note
	3/27	4	Remove LEDS on USB power, add gate resistor and capacitor to slow USB turn on & prevent power dip
	3/28	11	Add Push_Reset_L signal to FPGA
	3/29	13	Change DQS termination from midpoint to dual src
P3	4/24	13	Move DQS2 to pin J15 (P2-2)
		7	Add Schematic Text to explain built in LDOs.
		7	Change Ethernet Reset to be driven from FPGA. (P2-3)
		9	Add pull-up resistor on Push_Reset_L (P2-3)
		10	Remove R123 from FPGA_PROG_B Net.
		2	Changed Bus Name FPGA_GREEN[7:0] to FPGA_RED[7:0].
		7	Moved RJ45 LEDs to V3V3.
		7	Add no-load resistor to support KS8001L
		7	Add Clock Line from FPGA to replace Crystal
		7	Add pull-down resistor on ETH_RSTN.
		8	Add pull-down resistor on FPGA_CODEC_RESET
		9	Add EMI Filter and Reverse Protection Diode to Input Power.
		3	Add pull-down resistor on FPGA_USB_RESET_L
		3 & 6	Renamed VGA_RED, GREEN, and BLUE to be VGA_R, G, and B to avoid conflict with bus names.
		3	Removed FPGA_DDC_EN signal, tied high instead.
		12	Decreased the value of R129 and R130, and added 1uF to VREF generation circuit.
		3	Added buffers to HSYNC & VSYNC, Changed Series Term Value, and removed extraneous ESD Clamp.
		3	R27 & R29 are now pull-ups.
		5	Added 10uF Cap, 221ohm Resistor, and HEADSET_DET
		7 & 11	Eth det signal
		2	Added Polyfuse on DDC 5V
			Removed Debug Features throughout
		13	Changed DDR Clock Termination and added provision for LVCMOS signalling

Rev	Date	Pages	Description of Changes
P4	5/18		Moved some circuitry to lower board Added extensive power monitoring
P4	7/2/07		Released
	8/11/07	13	Added FET, R, and C to filter out red LED flash during reset.
		13	Added R148 to keep LM809 powered during use.
		13	Separated V2V5_REF and V3V3_REF.
		10	Added R149 on FPGA_CODEC_SCLK.
		17	Marked DDR Clock destination termination components as NI
P5	8/12/07		Released
P6	9/13/07		Released, only title block changes, as P6 was simply a layout change.
P7	11/17/07	5	USB ESD Changes
		3	Added more bypass on V3V3
A	11/19/07	3	Changed bypass scheme on VREG_1V8 to resemble NXP's reference design.
B	2/7/08	12	Connected DM lines, removed R83 and R34.
		12	Uninstalled (debug feature) FPGA Programmed LED to save cost
		3	Uninstall R156 to select proper voltage for USB controller. This was done on rev A, but was wrong in the schematic.
		2	Remove 0 ohm resistor R116, and tie VGA_AVDD rail directly to 3.3V.
C	6/19/08	4	Added 3 port HUB between NXP and external USB connectors.
		4	Added Maxim USB power switch with max Iout = 700ma
		10	Added control for new USB hub to previously unused FPGA pins
		3,4	Updated NXP USB Controller to TFBGA package
		4	Added pull-ups on Clk_En input of Hub and Pwr_En inputs of USB power switches. Removed filter cap on OCS3 input of NXP
		10	Added series R to 24MHz Clk output to USB hub. Added FS flag from USB hub.
C		3	Combined Rpack pull-ups on upper USB_D databus into a single pull-up to allow for via breakout space on board.
		4,10	Updated reference designators to ensure no overlap between Rev B and Rev C boms.
C1	8/11/08	4	Changed R501-503 to 221 ohms and tied to 5V Added R900-R903.
D	1/14/09	7	Added filter to RJ45 LEDs.
	1/14/09	13	Modified board to board connector pinout.

INSTALLED PROPERTY

All parts on this schematic are labeled with an "INSTALLED" property. The value is one of the following:

Null	Part is installed on the board
Blank	Part is installed on the board
NI	Footprint exists on the board, but part is not installed
PCB	Schematic symbol represents a feature of the PCB, no part goes at this location.
DBG	Installed in lab for debug purposes only. Removed for production.

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Title	Pano Upper Board	
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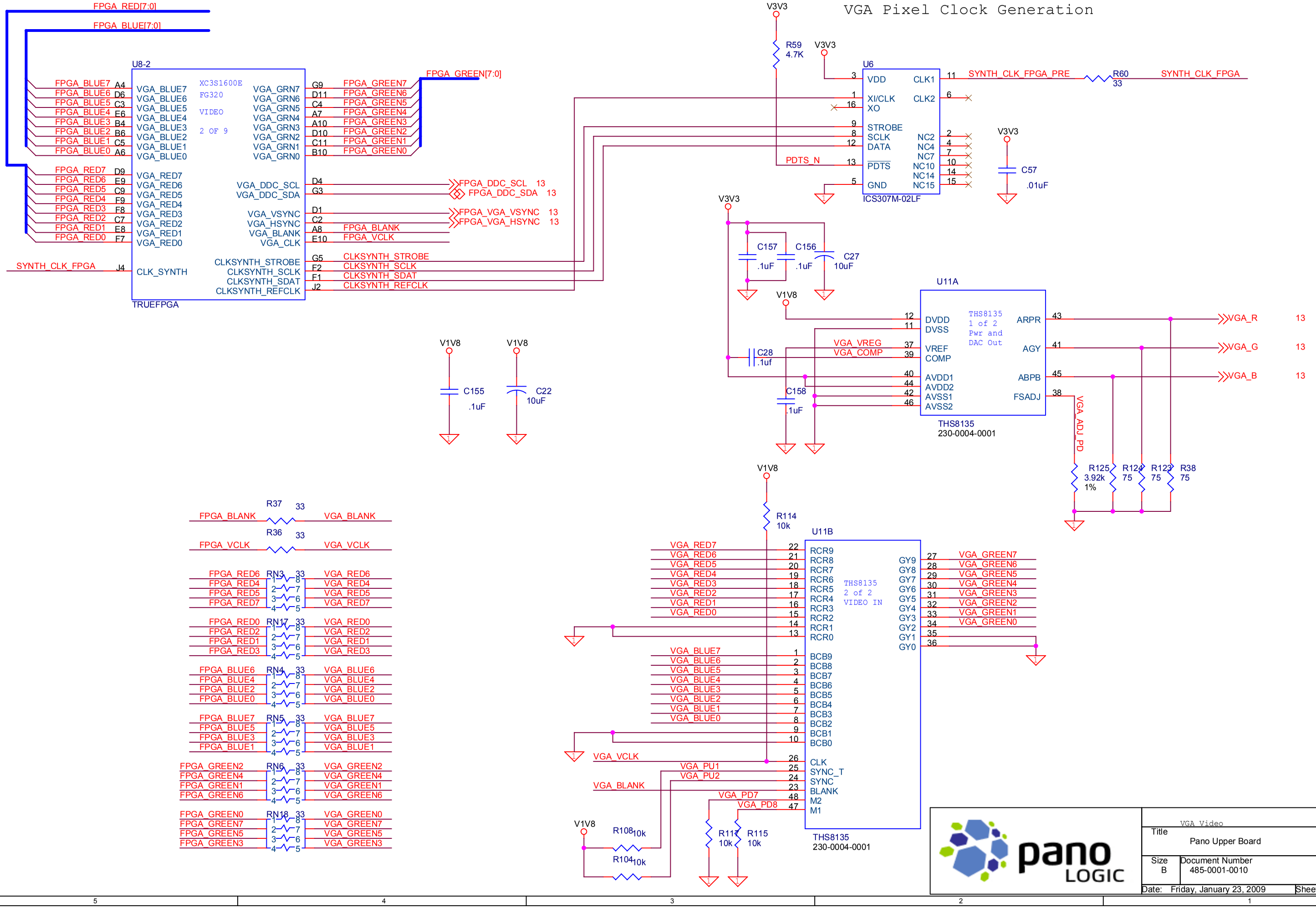
VGA Pixel Clock Generation



	VGA_Video		
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FPGA_USB_D[15:0]

U8-3

XC3S1600E
FG320

USB
3 OF 9

TRUEFPGA

U9-2

isp1760
lqfp128
2 of 3
host interface

ISP1760_LQFP128

U9-1

isp1760
lqfp128
1 of 3
Pwr

ISP1760_LQFP128

FPGA_USB_D15	V13	USB_D15	USB_A17	P9	FPGA_USB_A17	105	A17
FPGA_USB_D14	R9	USB_D14	USB_A16	R11	FPGA_USB_A16	103	A16
FPGA_USB_D13	V11	USB_D13/M1	USB_A15	U6	FPGA_USB_A15	102	A15
FPGA_USB_D12	U4	USB_D12	USB_A14	U13	FPGA_USB_A14	101	A14
FPGA_USB_D11	M10	USB_D11/M0	USB_A13	T5	FPGA_USB_A13	100	A13
FPGA_USB_D10	R13	USB_D10	USB_A12	R5	FPGA_USB_A12	98	A12
FPGA_USB_D9	P13	USB_D9	USB_A11	P6	FPGA_USB_A11	97	A11
FPGA_USB_D8	R14	USB_D8	USB_A10	R6	FPGA_USB_A10	96	A10
FPGA_USB_D7	T14	USB_D7	USB_A9	V5	FPGA_USB_A9	95	A9
FPGA_USB_D6	T16	USB_D6/VS0	USB_A8	V7	FPGA_USB_A8	93	A8
FPGA_USB_D5	M9	USB_D5	USB_A7	P7	FPGA_USB_A7	92	A7
FPGA_USB_D4	N9	USB_D4	USB_A6	N7	FPGA_USB_A6	91	A6
FPGA_USB_D3	V12	USB_D3	USB_A5	N8	FPGA_USB_A5	89	A5
FPGA_USB_D2	T15	USB_D2	USB_A4	P8	FPGA_USB_A4	87	A4
FPGA_USB_D1	U5	USB_D1	USB_A3	T8	FPGA_USB_A3	86	A3
FPGA_USB_D0	V6	USB_D0	USB_A2	R8	FPGA_USB_A2	84	A2
			USB_A1	N11	FPGA_USB_A1	82	A1
			USB_WR_N	P12	FPGA_USB_WR_PRE 33 R30		
			USB_RD_N	T12	FPGA_USB_RD_PRE 33 R28		
			USB_CS_N	R12	FPGA_USB_CS_PRE 33 R29		
			USB_IRQ	U14	1k R93		
			USB_RESET_N	P11	FPGA_USB_RESET_L		
			USB_REFCLK	K6	12MHZ_S 33 R84		
					USB_TEST3	117	TEST3
						113	NC1
					FPGA_USB_DACK	116	HC_DACK
					USB_FPGA_DREQ	114	HC_DREQ
						122	RESET_N
					USB_FPGA_IRQ		
					FPGA_USB_WR_L	108	WR_N
					FPGA_USB_RD_L	107	RD_N
					FPGA_USB_CS_L	106	CS_N
					CLK:12MHZ_USB 4		

DATA31	80
DATA30	78
DATA29	77
DATA28	76
DATA27	74
DATA26	73
DATA25	72
DATA24	70
DATA23	69
DATA22	68
DATA21	66
DATA20	65
DATA19	64
DATA18	62
DATA17	61
DATA16	60
DATA15	58
DATA14	57
DATA13	56
DATA12	54
DATA11	52
DATA10	51
DATA9	49
DATA8	47
DATA7	46
DATA6	45
DATA5	43
DATA4	42
DATA3	41
DATA2	39
DATA1	38
DATA0	37
IRQ	112
NC2	111

USB_PU_D_UPPER — R500 4.7k — V3V3

FPGA_USB_D15, FPGA_USB_D14, FPGA_USB_D13, FPGA_USB_D12, FPGA_USB_D11, FPGA_USB_D10, FPGA_USB_D9, FPGA_USB_D8, FPGA_USB_D7, FPGA_USB_D6, FPGA_USB_D5, FPGA_USB_D4, FPGA_USB_D3, FPGA_USB_D2, FPGA_USB_D1, FPGA_USB_D0

R67 4.7k VS0 — V3V3

R69 4.7k M0 — V3V3

R66 4.7k M1

R89 10k, R98 10k, R86 10k, R100 10k — V3V3

V3V3, V5V0

0 R155

0 R156 NI

C187 .1uF

R82 12.0k 1% ISP_RREF_1

R76 12.0k 1% ISP_RREF_2

R70 12.0k 1% ISP_RREF_3

RREF1, GND1_RREF, RREF2, GND2_RREF, RREF3, GND3_RREF

TEST7_VCC_C_IN — V3V3

VREG_1V8_1 — C186 10uF, C149 .1uF

VREG_1V8_2 — C122 10uF, C121 .1uF

VREG_1V8_3

VREG_1V8_4

VREG_3V3 — ISP_VREG_3V3 — C128 .1uF, C126 10uF

C138 .1UF, C86 .1uF

C180 .1uF — V3V3

C181 10uF — V3V3

C182 .1uF, C183 .1uF, C184 .1uF, C185 .1uF — V3V3

C114 10uF — V3V3

C135 .1uF, C88 .1uF, C129 .1uF, C72 .1uF, C133 .1uF — V3V3

C100 10uF — V3V3

C151 .1uF, C150 .1uF — V3V3

C140 .1uF — V5V0

C115 .1uF, C94 .1uF, C87 .1uF, C103 .1uF, C141 .1uF — V3V3

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Usb Host Side Interface

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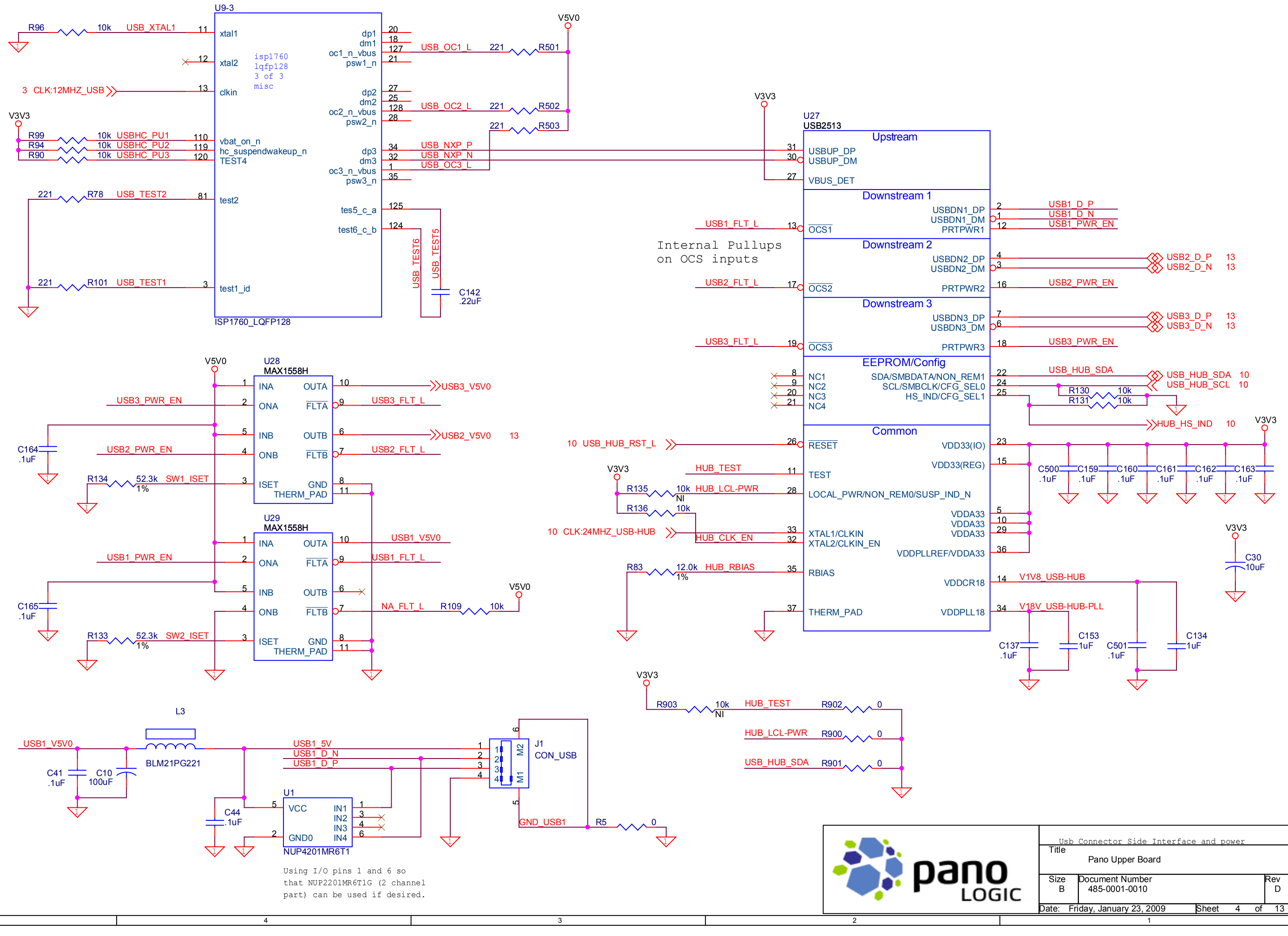
U9-3
isp1760
lqfp128
3 of 3
misc
ISP1760_LQFP128
R96 10k USB_XTAL1
3 CLK:12MHZ_USB
R99 10k USBHC_PU1
R94 10k USBHC_PU2
R90 10k USBHC_PU3
221 R78 USB_TEST2
221 R101 USB_TEST1
C142 .22uF
V5V0
V3V3
R501 R502 R503 221
USB_OC1_L
USB_OC2_L
USB_NXP_P
USB_NXP_N
USB_OC3_L
U27
USB2513
Upstream
Downstream 1
Downstream 2
Downstream 3
EEPROM/Config
Common
USBUP_DP
USBUP_DM
VBUS_DET
USBDN1_DP
USBDN1_DM
PRTPWR1
USB1_FLT_L
USB1_D_P
USB1_D_N
USB1_PWR_EN
Internal Pullups
on OCS inputs
USBDN2_DP
USBDN2_DM
PRTPWR2
USB2_FLT_L
USB2_D_P 13
USB2_D_N 13
USB2_PWR_EN
USBDN3_DP
USBDN3_DM
PRTPWR3
USB3_FLT_L
USB3_D_P 13
USB3_D_N 13
USB3_PWR_EN
NC1
NC2
NC3
NC4
SDA/SMBDATA/NON_REM1
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
USB_HUB_SDA
USB_HUB_SCL 10
R130 10k
R131 10k
HUB_HS_IND 10
10 USB_HUB_RST_L
RESET
HUB_TEST
TEST
R135 10k HUB_LCL-PWR NI
R136 10k
LOCAL_PWR/NON_REM0/SUSP_IND_N
10 CLK:24MHZ_USB-HUB
XTAL1/CLKIN
XTAL2/CLKIN_EN
HUB_CLK_EN
R83 12.0k HUB_RBIAS 1%
RBIAS
THERM_PAD
VDD33(IO)
VDD33(REG)
VDDA33
VDDA33
VDDA33
VDDPLLREF/VDDA33
VDDCR18
VDDPLL18
V1V8_USB-HUB
V18V_USB-HUB-PLL
C500 .1uF
C159 .1uF
C160 .1uF
C161 .1uF
C162 .1uF
C163 .1uF
C30 10uF
C137 .1uF
C153 1uF
C501 .1uF
C134 1uF
U28
MAX1558H
U29
MAX1558H
INA
ONA
INB
ONB
ISET
OUTA
FLTA
OUTB
FLTB
GND
THERM_PAD
USB3_V5V0
USB3_FLT_L
USB2_V5V0 13
USB2_FLT_L
C164 .1uF
R134 52.3k SW1_ISET 1%
USB1_V5V0
USB1_FLT_L
C165 .1uF
R133 52.3k SW2_ISET 1%
NA_FLT_L
R109 10k
L3
BLM21PG221
C41 .1uF
C10 100uF
USB1_5V
USB1_D_N
USB1_D_P
J1
CON_USB
M1
M2
U1
NUP4201MR6T1
VCC
GND0
IN1
IN2
IN3
IN4
C44 .1uF
GND_USB1
R5 0
R903 10k NI HUB_TEST R902 0
HUB_LCL-PWR R900 0
USB_HUB_SDA R901 0
Using I/O pins 1 and 6 so
that NUP2201MR6T1G (2 channel
part) can be used if desired.
pano LOGIC
Usb Connector Side Interface and power
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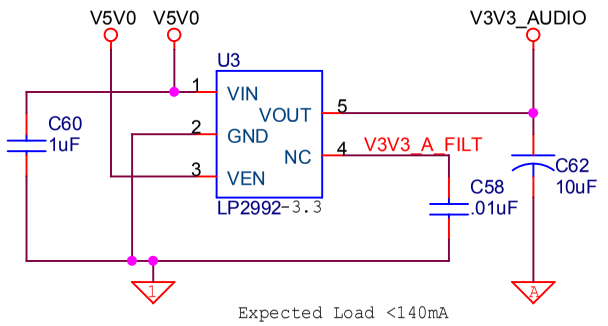
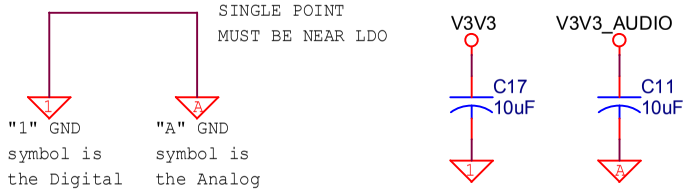
SHLD PINS NOT USED FOR 3534

3.3V supply
up to 250mA



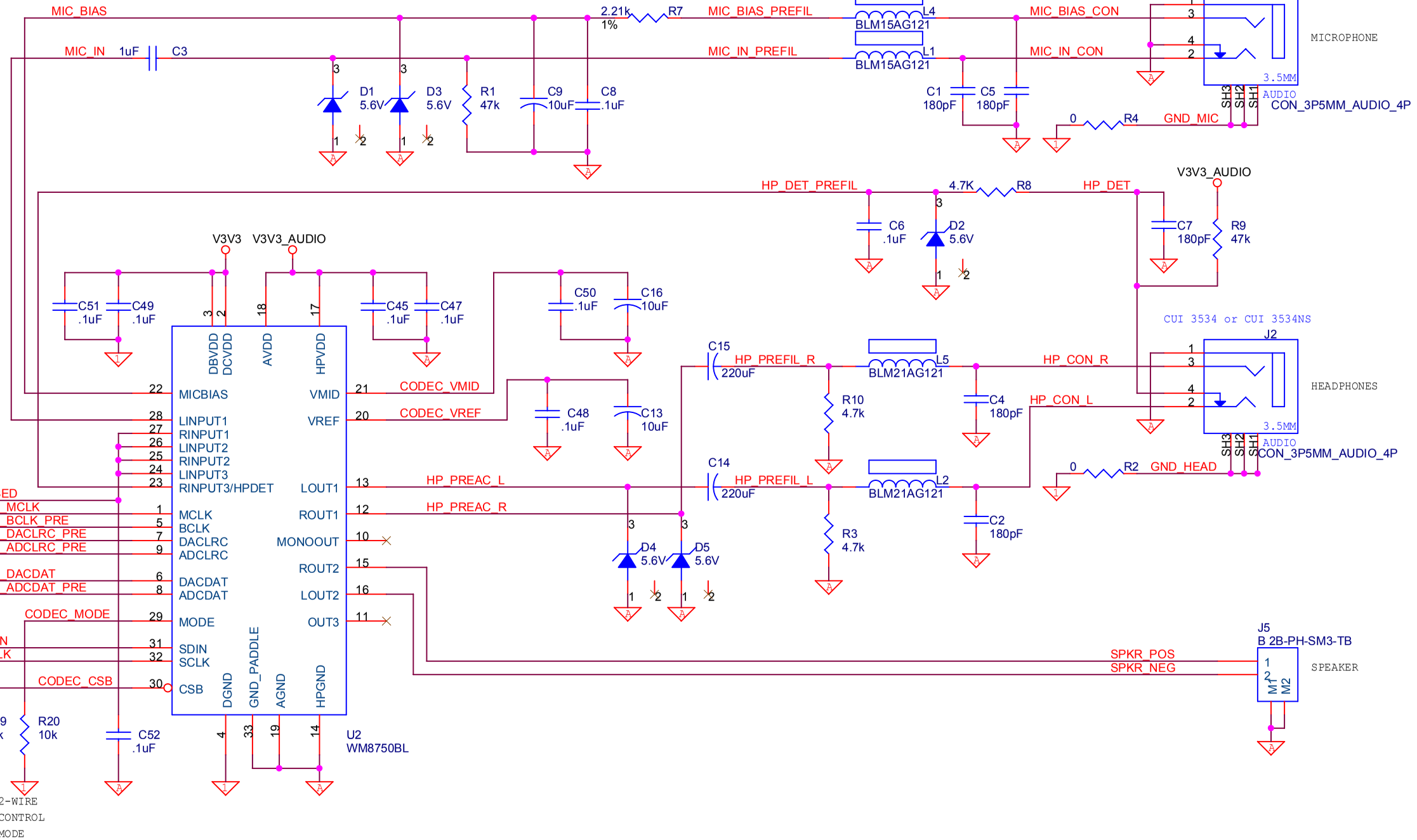
Expected Load <140mA

CONNECT AUDIO GND TO
DIGITAL GND AT A
SINGLE POINT
MUST BE NEAR LDO



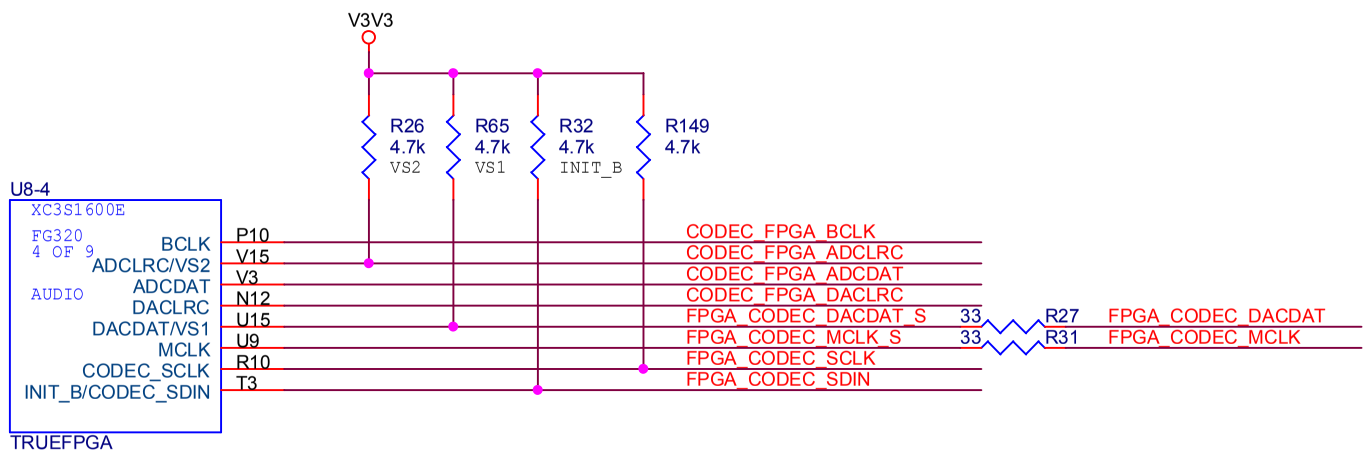
"1" GND symbol is the Digital Ground

"A" GND symbol is the Analog Ground



NOTES:

1. Layout: Read Power Supply notes on page 46 of WM8750BL data sheet and refer to notes for Figure 50.
2. HPSWEN bit should be set to a 1 HPSWPOL bit should be set to 0.
3. 220uF caps should be 6.3V Aluminum Electrolytics.
4. Check that loading on HP_DET_PREFIL doesn't pull this signal low when plug is inserted into the headphone jack.



lm4550_audio_circuitry
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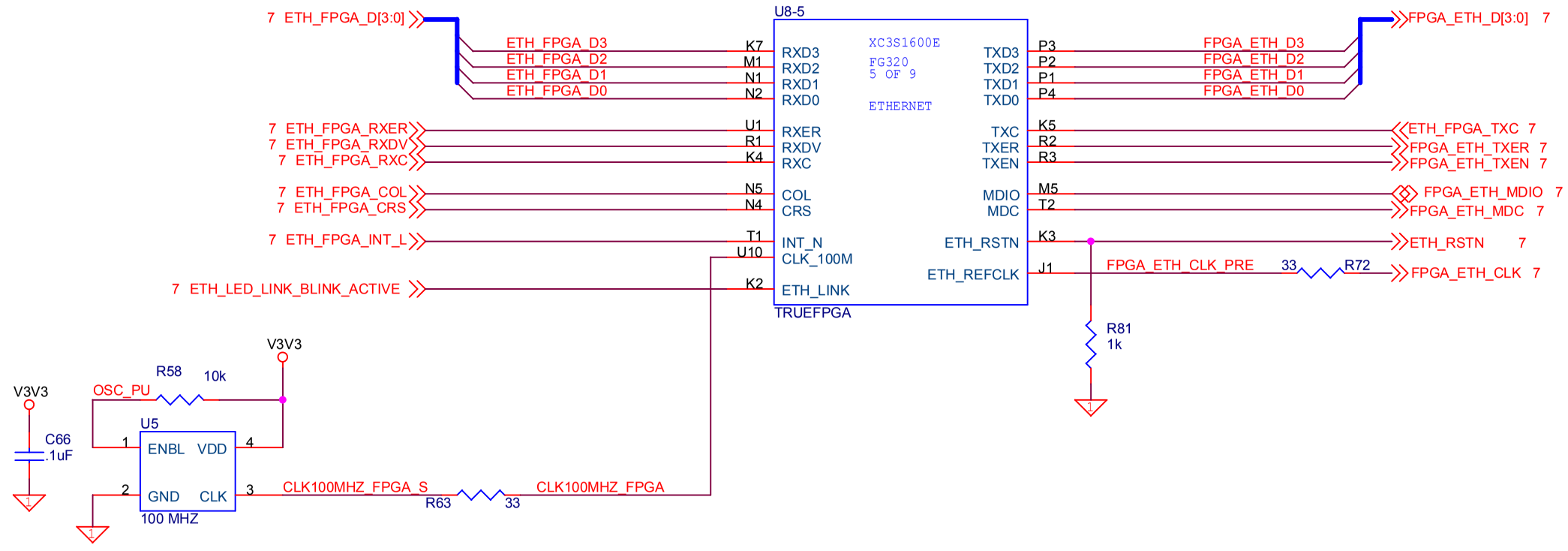

Micrel 8721/8001 ethernet transceiver

Title: Pano Upper Board		
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U12 can be one of two PHY chips: KS8721BL48-LQFP or KSZ8001L.

If it is the KS8721BL, then there is an integrated LDO that generates 2.5V from 3.3V. Input on pin 7 & 24, output on pin 38. This part requires 2.5V on pins 31, 42, 13, and 47, as well as the transformer center taps. It requires 3.3V on 7 & 24.

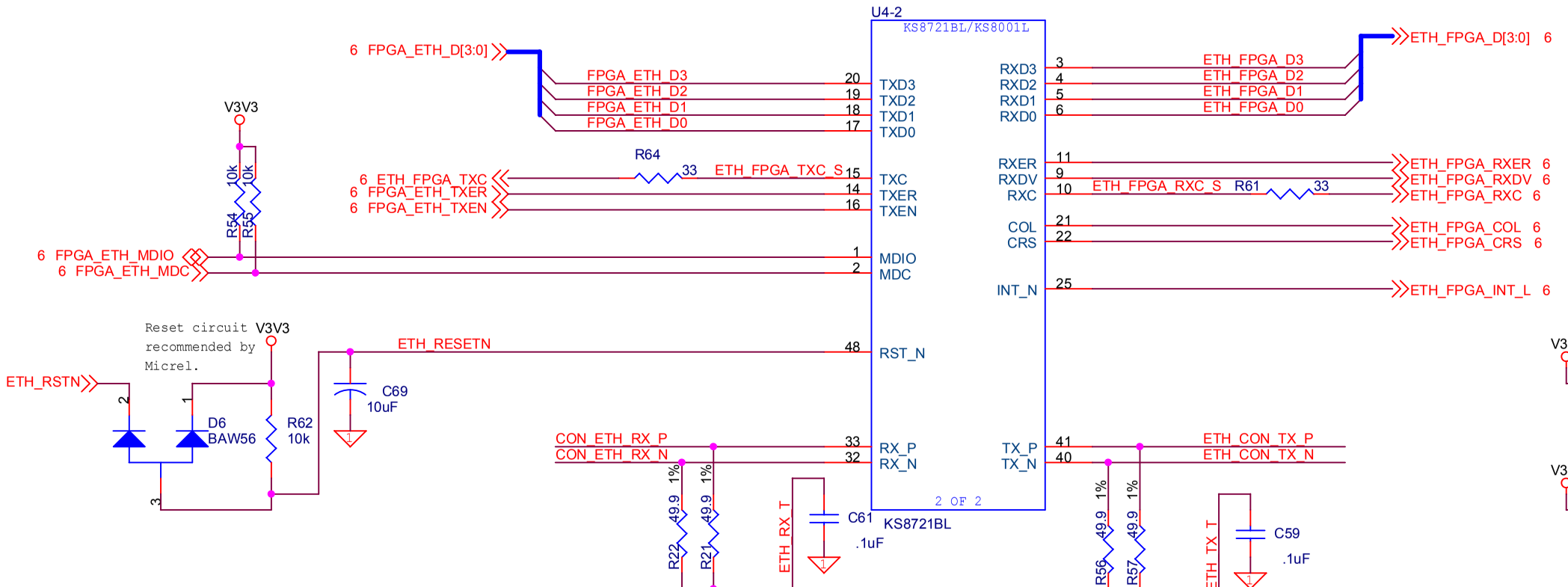
If it is the KSZ8001L, then there is an integrated LDO that generates 1.8V from 3.3V. Input on pin 7 & 24, output on pin 13. This part requires 1.8V on pins 31 & 47. 42 is NC. It requires 3.3V on 7, 24, and 38 and the transformer center taps.

Loading Options:

KS8721BL48-LQFP:
Load R58.
Unload R301.

KSZ8001L:
Unoad R58.
Load R301.

Pin	Strapping Options	Normal Pin Function	Default if floated	Strap
6,5,4,3	Phyad[4:1]	RXD[0:3]	0000	none
25	Phyad0	INT_N	1	none
9	Pcs_Lpbk	RXDV	disable	none
11	Iso	RXER	disable	none
21	Rmii	COL	disable	none (DNS)
22	Rmii_Btb	CRS	disable	none
27	Spd100	LED1	100m	none
28	Duplex	LED2	full	none
29	Nwayen	LED3	enable	none
30	PD_N	PD_N	power up	none



Micrel 8721/8001 ethernet transceiver

Title: Pano Upper Board

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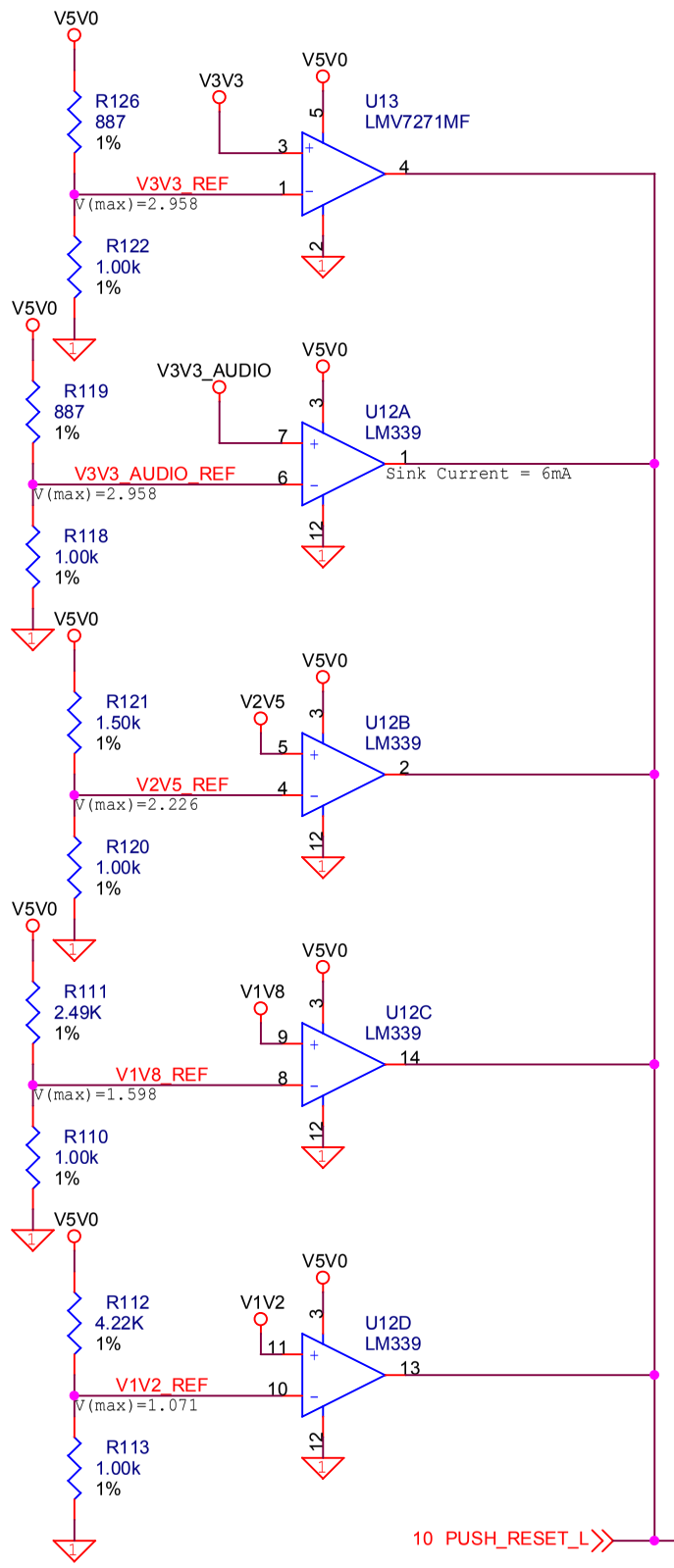
Assume Vin is up to 10% high (5.5V), bottom resistor is 1% high and top resistor is 1% low when calculating thresholds. Thresholds are set 5% below nominal voltage.

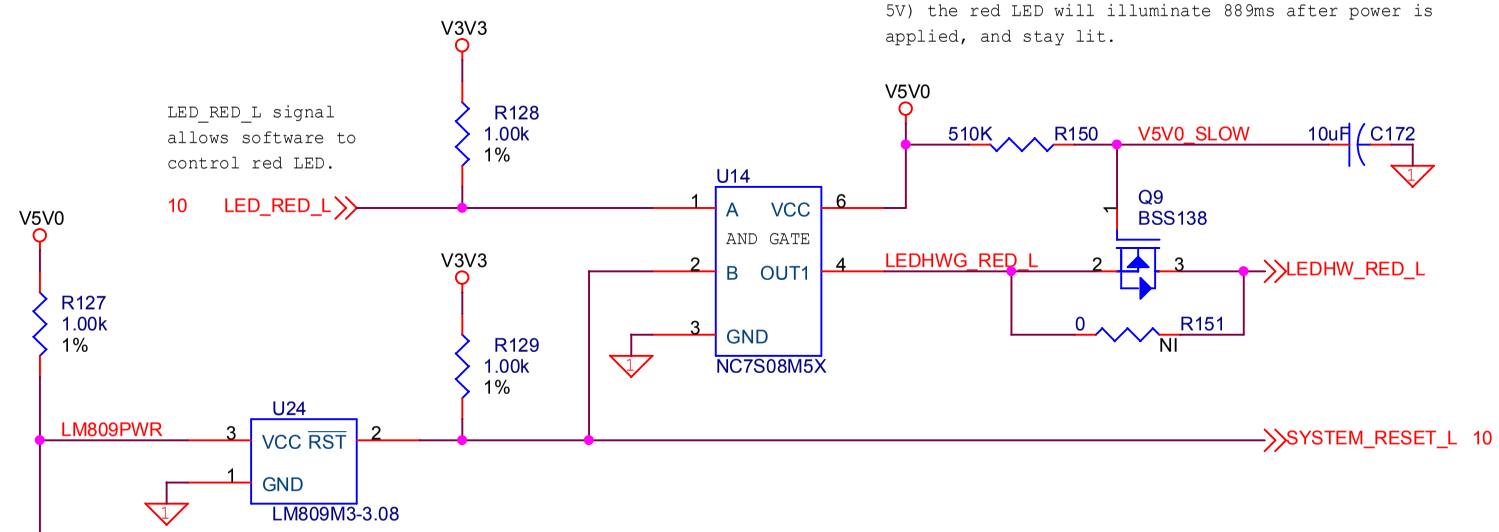
5V0V	Other Rails		PUSH_RESET_L	SYSTEM_RESET_L	LED_RED_L	LEDHW_RED_L	LED_ON?
OK	OK		Low (Forced by FPGA)	Low	High	High after 140uS	No (only for 140uS)
OK	OK		High	High after 140uS	High	High after 140uS	No (only for 140uS)
OK	BAD		Low	Low	High	Low	Yes
OK	OK		X	X	Low	Low	Yes
BAD	X		X	X	Low	Low	No



System Reset and Power Rail Monitoring

BSS138 will not turn on until VGS>800mV
V5V0_SLOW won't reach 800mV until at least 889ms after power on.
This ensures that there is no flash of the red LED at power on.
If there is a fault in one of the power supplies (other than 5V) the red LED will illuminate 889ms after power is applied, and stay lit.

LED_RED_L signal allows software to control red LED.



R127/R148 Voltage divider keeps the LM809 powered so that it's output will be guaranteed.

PUSH_RESET_L signal allows software to reset the entire client.

Title	Power and Reset Pano Upper Board		
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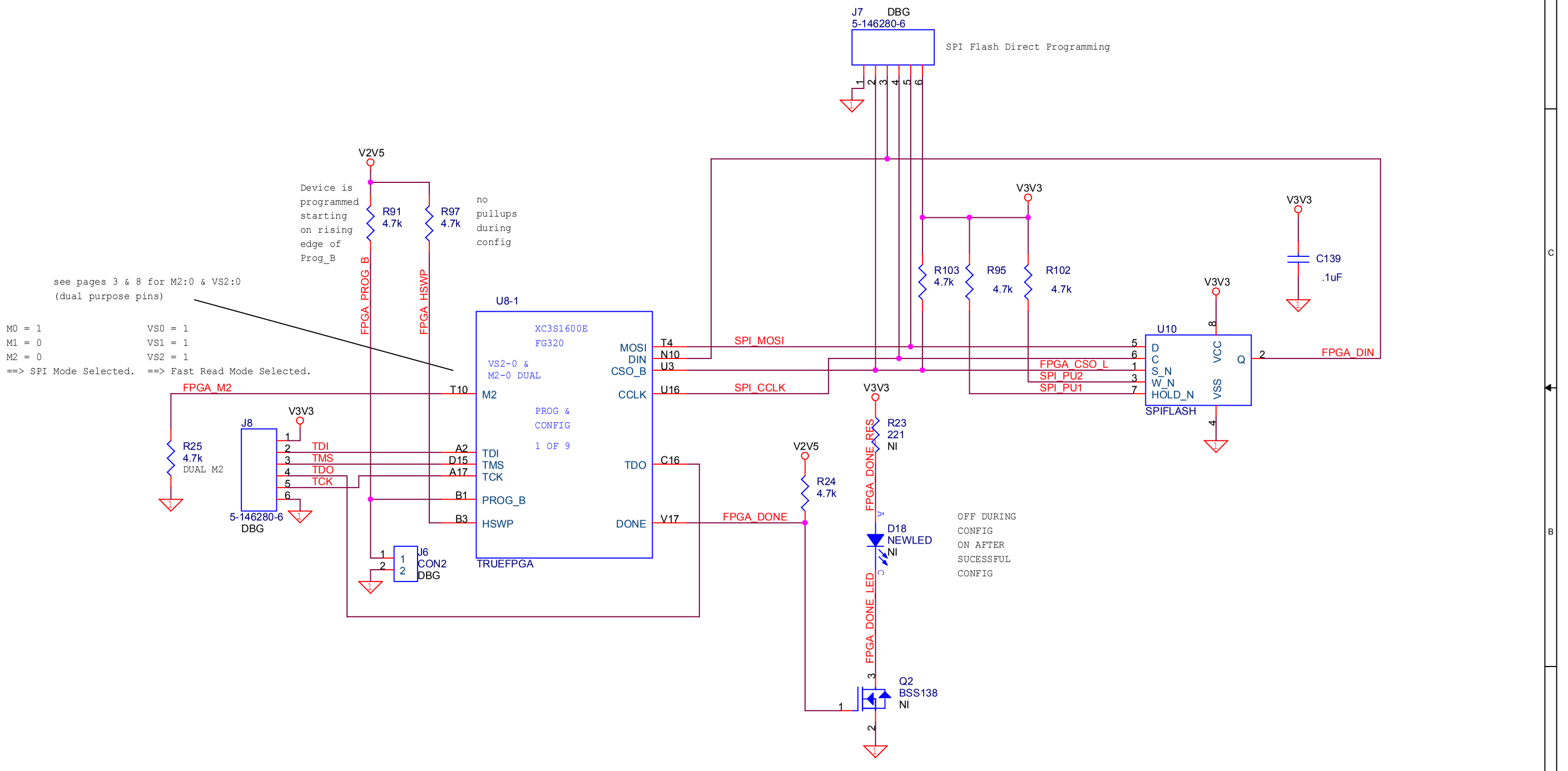

Title	FPGA FLASH, PROGRAM HEADER, AND CONFIGURATION Pano Upper Board	
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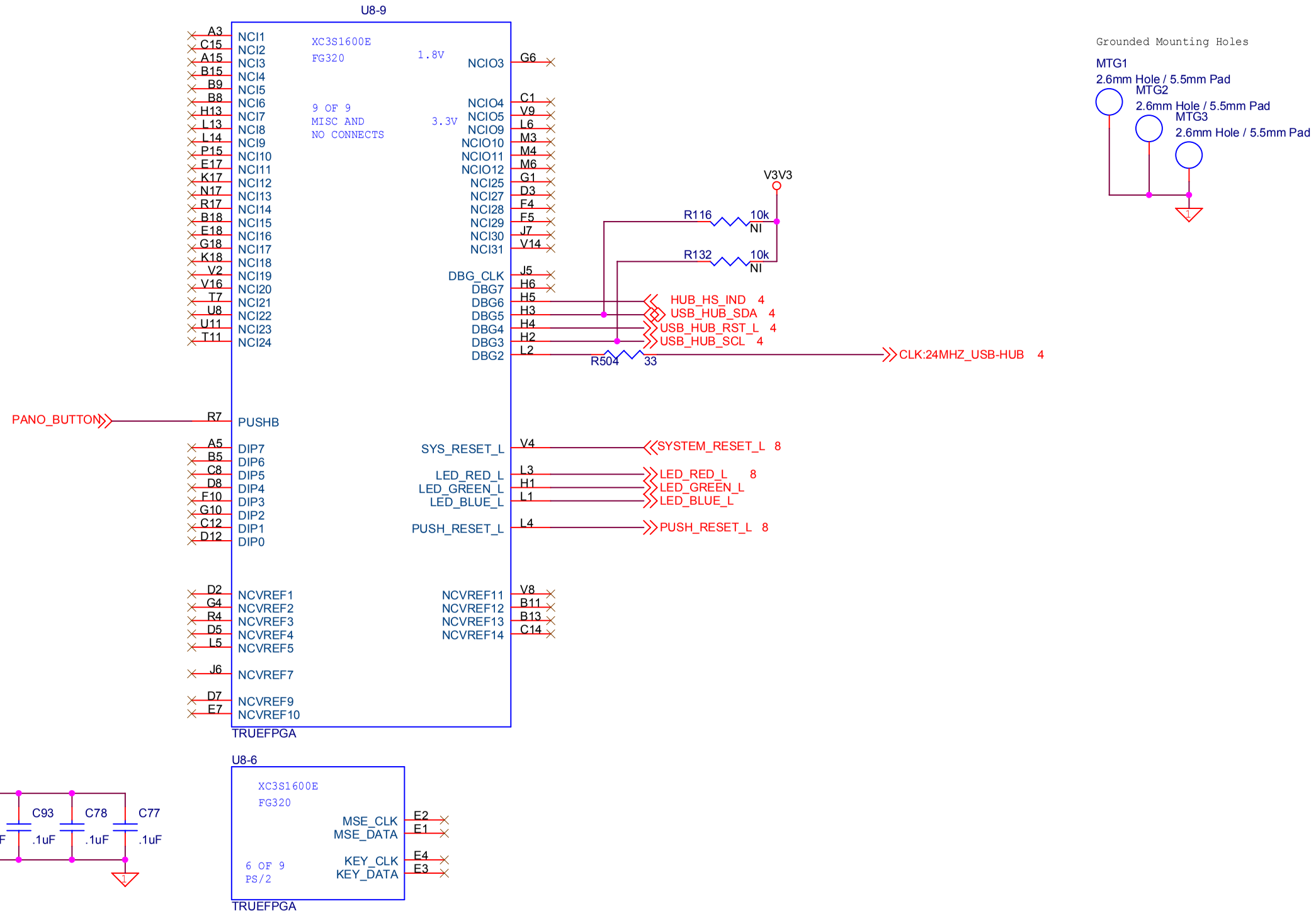

CLK SYNTHESIZER, DEBUG, LEDS

Title: Pano Upper Board

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FPGA power and decoupling

xilinx recommendation is approx 1 cap per power pin, with 80% of the caps being high frequency (.1uF or .01uF).

.1uF parts are preferred since we are able to get them in 0402 packages as opposed to Xilinx app notes which assume .1uF must be in 0603 package.

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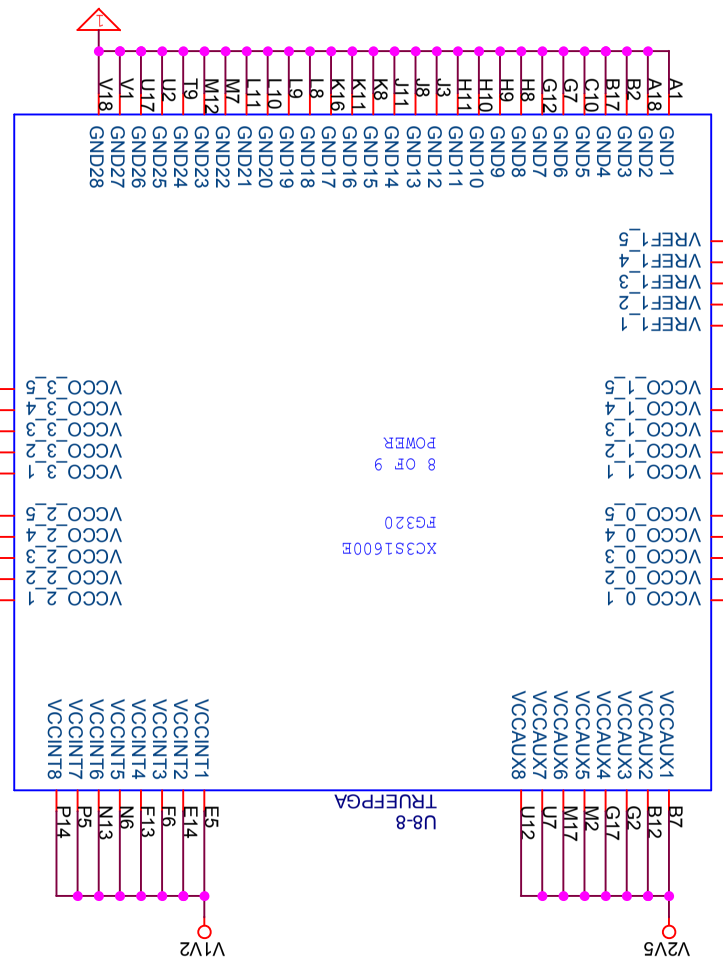
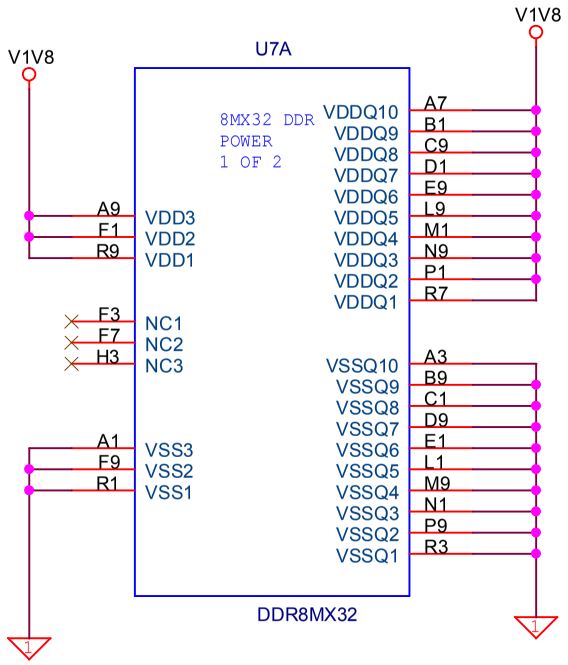
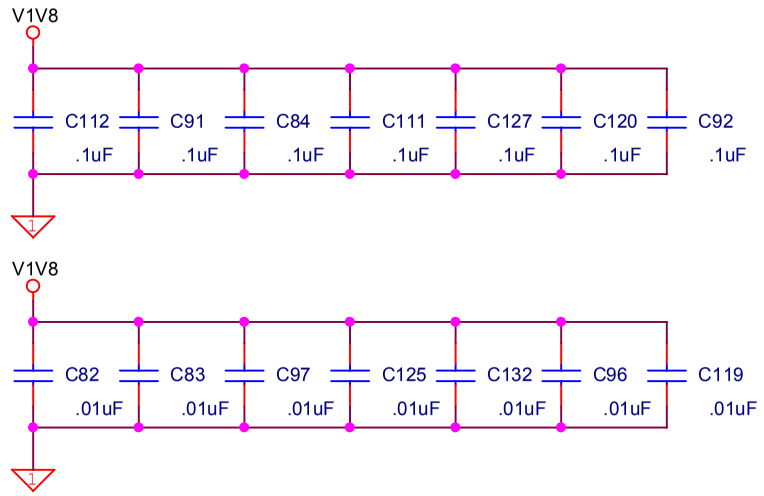
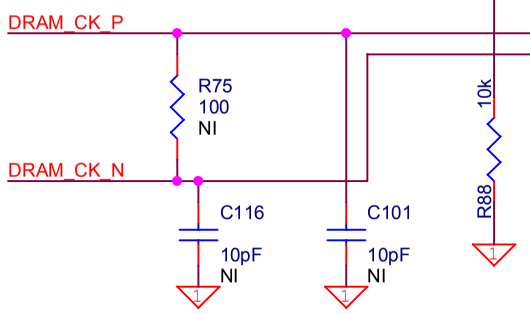
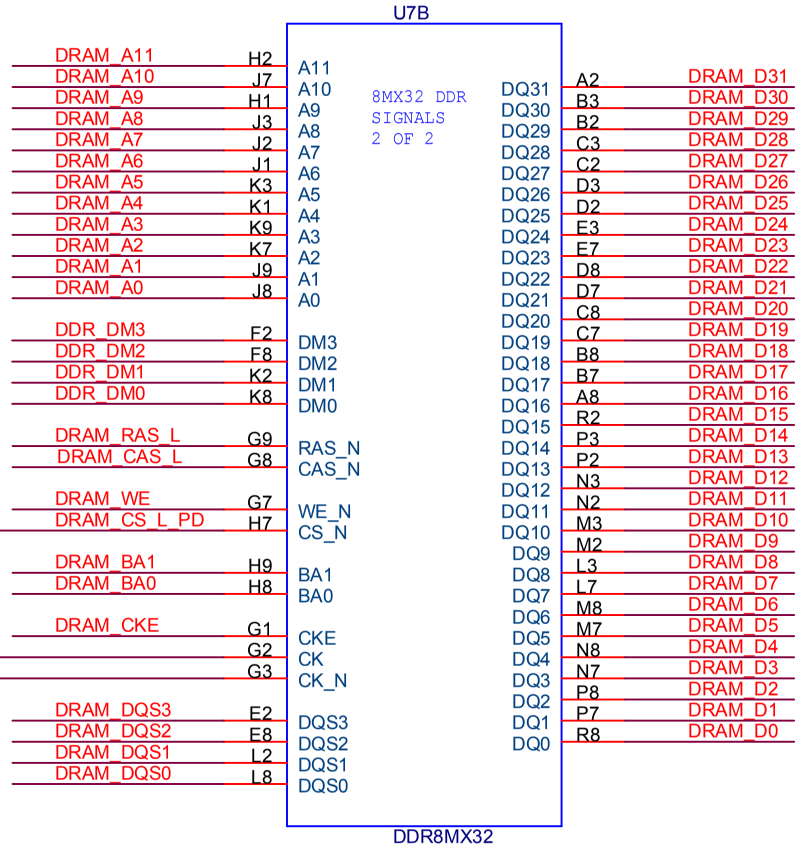
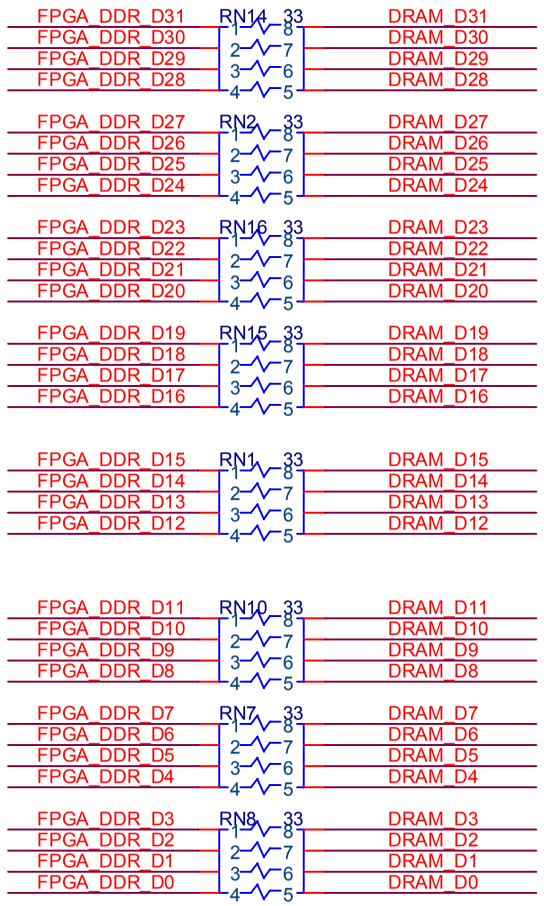




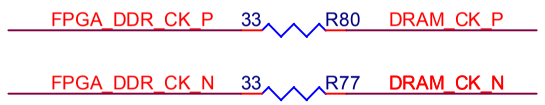


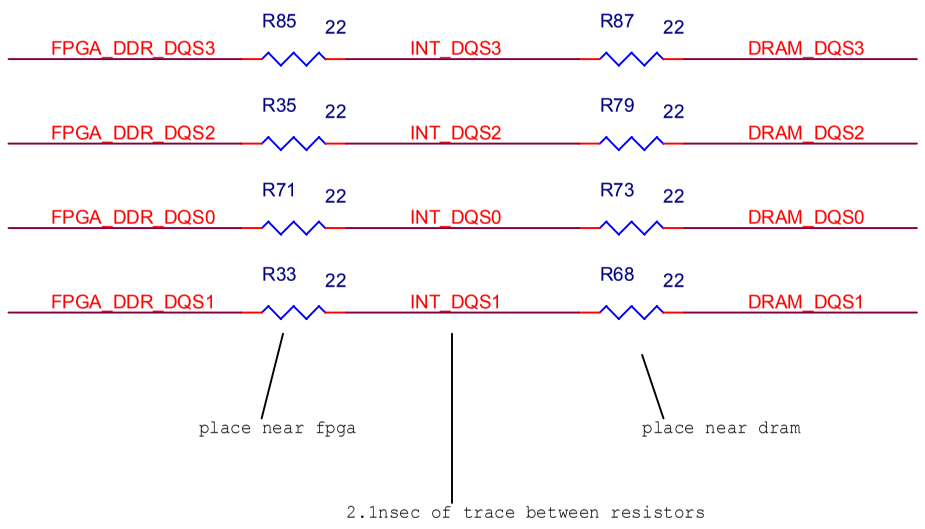


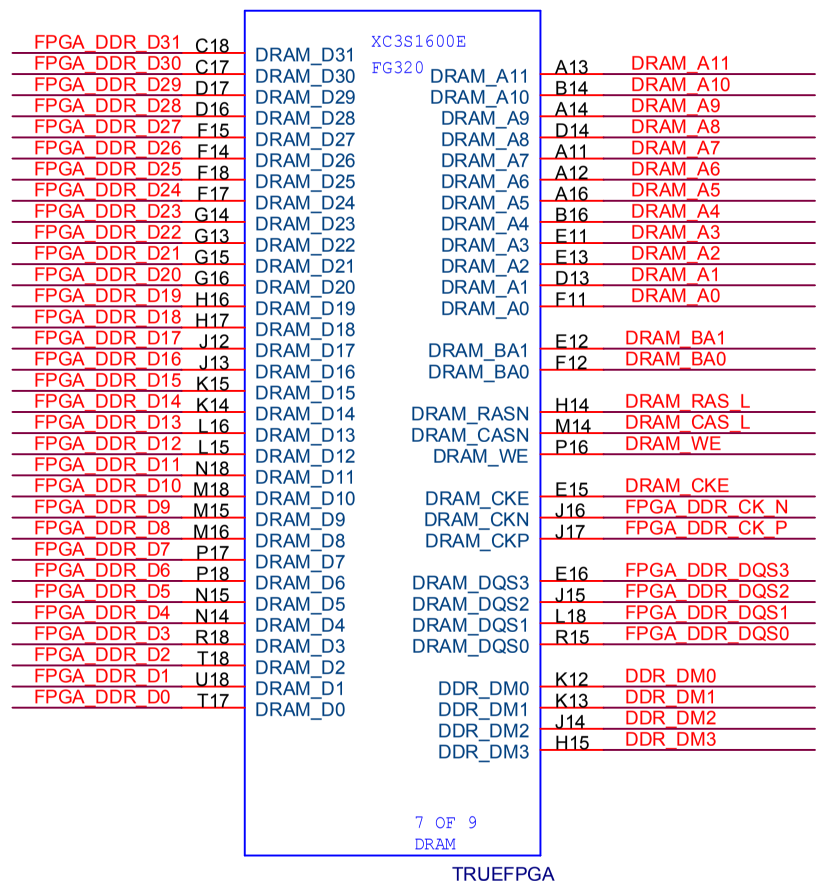




these rpacks need to be swapped as needed in layout







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FPGA to DRAM		
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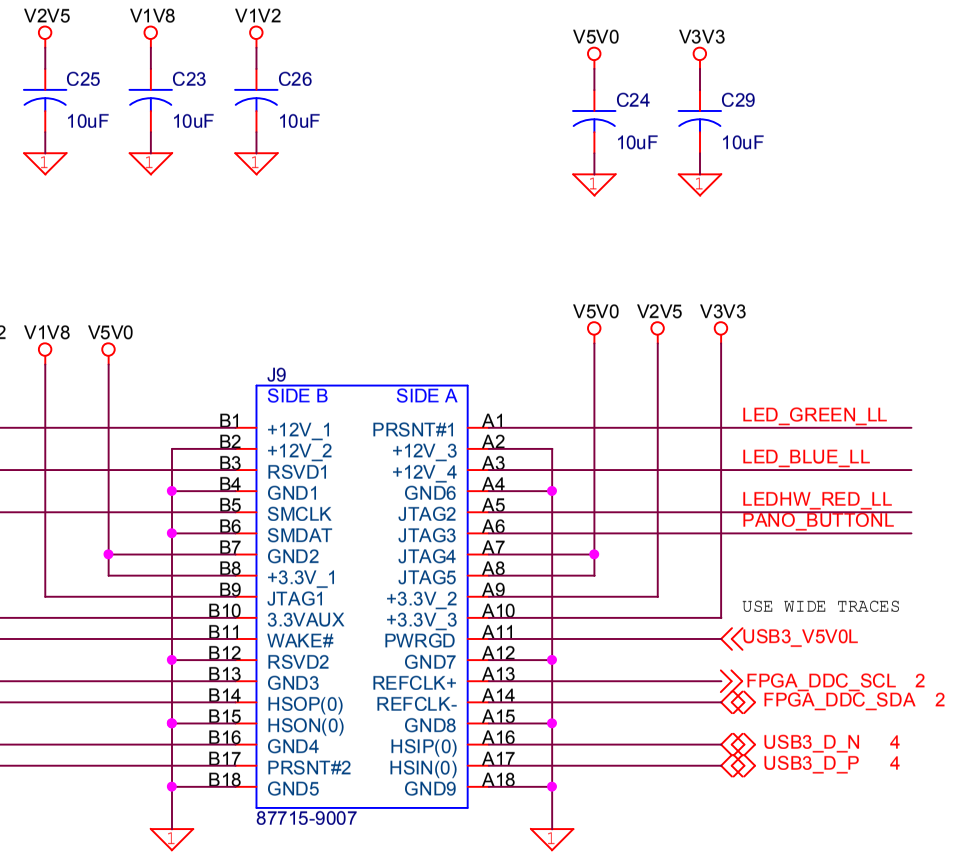

This is a PCI-E x1 Connector being used for our purposes. Pin names are PCI-E names, and are irrelevant for the TrueClient Design.

Connection To Lower Board

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